HPC CHALLENGE

http://icl.cs.utk.edu/hpcc/

PROJECT GOALS

To examine the performance of HPC architectures using kernels with more challenging memory access patterns than High Performance Linpack (HPL)
HPL works well on all architectures -- even cache-based, distributed memory
multiprocessors due to:
1. Extensive memory reuse
2. Scalability with respect to the amount of computation
3. Scalability with respect to the communication volume
4. Extensive optimization of the software

To augment the TOP500 list

To provide benchmarks that bound the performance of many real applications as a function of memory access characteristics – e.g. spatial and temporal locality

HOW IT WORKS

Single program to download and run
Simple input file similar to HPL input

Base Run and Optimization Run
Base run must be made
Optimized run allowed to replace certain routines

Results upload via web site (http://icl.cs.utk.edu/hpcc/)

HTML table, Excel spreadsheet, and XML generated with performance results
No ranking

THE HPC CHALLENGE COMPONENTS

HPL
The Linpack TPP benchmark, which measures the floating point rate of execution for solving a linear system of equations

STREAM
A simple synthetic benchmark program that measures sustainable memory bandwidth (in GB/s) and the corresponding computation rate for simple vector kernel

RandomAccess
Measures the integer update rate of random locations in large memory array

PTRANS
(Parallel matrix transpose) Excercises the communications where pairs of processors communicate with each other simultaneously

FFT
(Fast Fourier Transform) Calculates discrete Fourier transfrom of one-dimensional complex data

b_eff
(Effective bandwidth benchmark) A set of tests to measure the latency and bandwidth of a number of simultaneous communication patterns

THE RESULTS

Computer	HPL	PTRANS	STREAM - single CPU				*STREAM				RandomAccess			Latency		Bandwidth		
			Copy	Scale	Add	Triad	Copy	Scale	Add	Triad	Single CPU	*	MPI	Ping Max.	Random Ring	Ping Min.	Random Ring	Natural Ring
System/Procs	TFlop/s	GB/s	GB/s	GB/s	GB/s	GB/s	GB/s	GB/s	GB/s	GB/s	Gup/s	Gup/s	Gup/s	usec	usec	GB/s	GB/s	GB/s

HPCS
ICL UT INNOVATIVE COMPUTING LABORATORY
THE UNIVERSITY of TENNESSEE Computer Science Department
CITR CENTER FOR INFORMATION TECHNOLOGY RESEARCH
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Jack Dongarra and Piotr Luszczek of the Innovative Computing Lab (ICL) at the University of Tennessee will announce the new release of a benchmark suite — the HPC Challenge Benchmarks — at SC2004 in Pittsburgh (6-12 November 2004). Jack Dongarra describes the goals of the HPC Challenge Benchmarks: "The HPC Challenge Benchmarks will examine the performance of HPC architectures using kernels with more challenging memory access patterns than just the High Performance Linpack (HPL) benchmark used in the Top500 list. The HPC Challenge Benchmarks are being designed to augment the Top500 list, provide benchmarks that bound the performance of many real applications as a function of memory access characteristics — e.g., spatial and temporal locality, and provide a framework for including additional benchmarks."

HPL performs well on many architectures, including cache-based, distributed memory multiprocessors, and the measured performance may not be representative of a wide range of applications like adaptive multi-physics simulations used in weapons and vehicle designs and weather and climate models. HPL is more compute friendly than these applications because it has more extensive memory reuse in the Level 3 BLAS-based calculations than the physics simulations models. HPL is also highly scalable with respect to both the amount of computation and the communication volume.

David Nelson (NITRD), a leader of the High End Computing (HEC) Revitalization Task Force (HECRTF), emphasized the need for benchmarks that test memory performance:

"Not only does the Japanese Earth Simulator outperform the top American systems on the Top500 list, if you look at the differences in performance on John McCalpin's STREAM TRIAD benchmark (Level 1 BLAS), the disparity in performance is significantly greater. The Earth Simulator outperforms the ASCI Q by a factor of 4.64 on HPL. Meanwhile, the higher bandwidth memory and interconnect systems of the Earth Simulator are clearly evident as it outperforms ASCI Q by a factor of 36.25 on STREAM TRIAD."

The HPC Challenge Benchmark suite includes the following kernels in its current release:

HPL: high spatial and temporal locality (authored by Antoine Petitet and R. Clint Whaley)

STREAM: high spatial locality and low temporal locality (stride 1 memory access) on a local processor (authored by John McCalpin)

RandomAccess: random memory access with low spatial and temporal locality (contributed by DARPA HPCS)

PTRANS ($A = A + B^T$): high spatial locality and low temporal locality with a matrix transpose to measure system bisection bandwidth (from ParkBench suite)

FFT (Fast Fourier Transform): low spatial and high temporal locality (authored by Daisuke Takahashi)

Interprocessor Bandwidth and Latency measurements (authored by Rolf Rabenseifner)

A portable MPI-based version of the HPC Challenge Benchmarks is also publicly available. After the benchmark is run on a computer the results can be electronically posted to a web site run by ICL where the results will be displayed in HTML form with an Excel spreadsheet and XML file both available. If a site desires to modify the code to optimize performance on their system, the site can post optimized results after posting results for the base version of the benchmark. Detailed information on the run rules and additional information can be found on the benchmark website.

Development of the HPC Challenge Benchmarks is being funded by the Defense Advanced Research Projects Agency (DARPA) High Productivity Computing Systems (HPCS) Program. Robert Graybill is the HPCS program manager. "We are interested in not only improved performance, but also ease of programming. These two combined is what will give us the productivity that the national security community needs. The HPCS program is developing activity and purpose benchmarks to allow developers and users to accurately evaluate emerging HPC systems. The HPC Challenge Benchmarks are the first major release of the activity or performance oriented benchmarks."

Jack Dongarra will introduce the HPC Challenge Benchmarks at The SC2004 Panel session, Friday, 12 November 2004, 10:30pm - 12:00pm, room 317-318. Additional information on the HPC Challenge Benchmarks can be found on the HPCC website.

ICL UT
Innovative Computing Laboratory

VISIT WITH THE ICL TEAM AT THE ORNL BOOTH AT SC2004