## INVE COMPUTING LABORATORY

PaRSEC is a generic framework for architecture aware scheduling and management of micro-tasks on distributed many-core heterogeneous

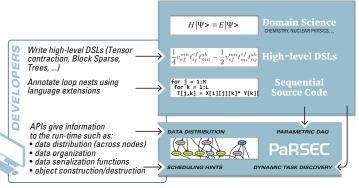
architectures. Applications we consider can be expressed as a Direct Acyclic Graph of tasks with labeled edges designating data dependencies. DAGs are represented in a compact problem-size independent format that can be queried on-demand to discover data dependencies in a totally distributed fashion. PaRSEC assigns computation threads to the cores, overlaps communications and computations and uses a dynamic, fully-distributed scheduler based on architectural features such as NUMA nodes and algorithmic features such as data reuse.

## **FEATURES**

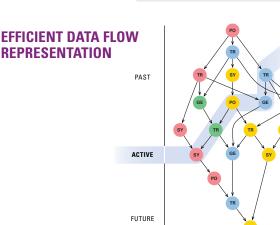
Supports Distributed Heterogeneous Platforms Sustained Performance NUMA & Cache Aware Scheduling State-of-the-art Algorithms Capacity Level Scalability Performance Portability Implicit Communication **Communication Overlapping** 

Node2

## **PaRSEC TOOLCHAIN**



Input serial codes are converted automatically by the PaRSEC compiler into the task Dataflow representation which can also be edited by the programmer. The **Dataflow compiler** generates the stubs that, along with the **Data distribution** provided by the programmer via Domain Specific Extensions, the Application code & Codelets, the Runtime and relevant libraries are linked by the system compiler to generate the executable that will run on a heterogeneous distributed memory supercomputer.



PaRSEC uses a symbolic, problem size independent representation to express the Directed Acyclic Graph (DAG) of the Dataflow of a program. As a result, at runtime, successors and predecessors of any given task can be evaluated independently, without exploring portions of the DAG pertaining to tasks localized on other nodes. Furthermore, the whole DAG is never **unfolded**, and only the set of locally active tasks resides in the memory at any given time.

## **APPLICABILITY DOMAINS**

