

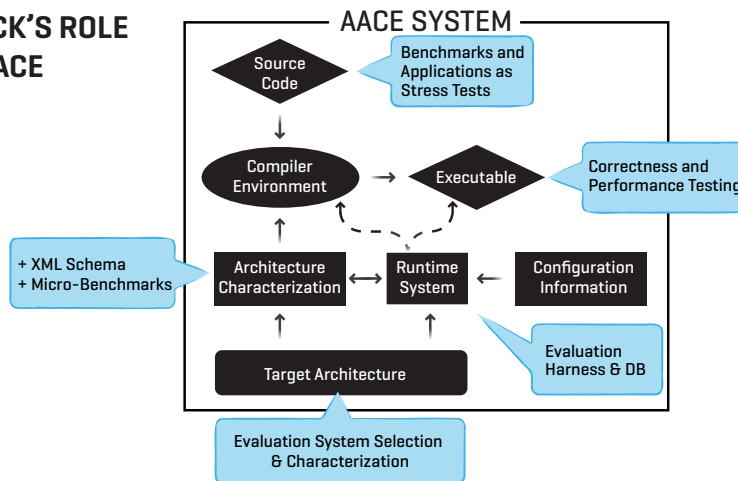
BLACKJACK



Modern computing system architectures change rapidly and exhibit high levels of complexity and heterogeneity. Developing compilers that can boost productivity while producing efficient code for these rapidly evolving targets is a difficult challenge that most existing compiler systems are unable to address in a comprehensive way. AACE [Architecture-Aware Compiler Environment] is a DARPA project that aims to produce modular compilers that can discover their environment and automatically adapt to it, so that it can efficiently optimize programs without involving a user's expertise.

Blackjack, as part of the AACE program, addresses the problem of characterizing target architectures in a rigorous and systematic way, provides a comprehensive list of benchmarks and applications that can stress and evaluate the AACE compilers, and assess the productivity benefits of such compiler systems.

BLACKJACK'S ROLE WITHIN AACE



BLACKJACK'S APPROACH IS ORGANIZED ALONG SIX THRUSTS:

- 1 Metrics
- 2 Specification of Metadata for Compiler Configuration and System Characterization
- 3 Benchmark and Application Evaluation Suite
- 4 Evaluation Harness and Database
- 5 Evaluation System Selection and Characterization
- 6 Prototype Evaluations

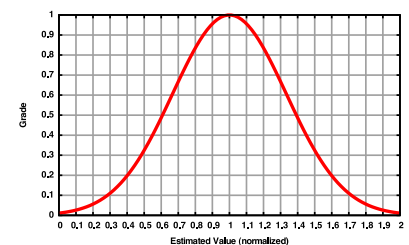
CHARACTERIZATION EVALUATION

Binary Grade: Fail or Pass

Critical Characteristics with integer values

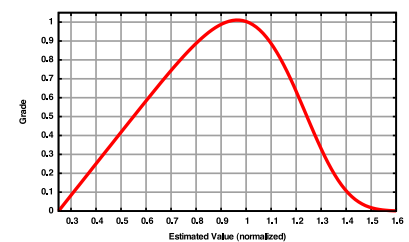
Normal distribution:

Latencies / Bandwidths



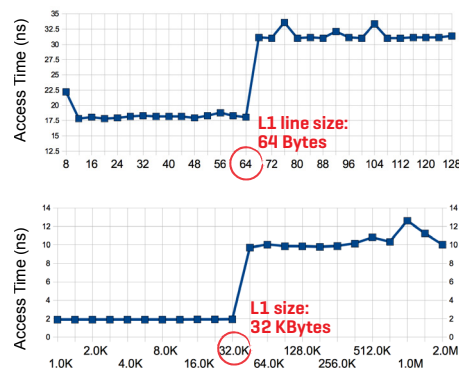
Skewed curve:

Values that are better to underestimate than overestimate



SYSTEM CHARACTERIZATION

L1 Cache Discovery Example



Characterization File Example

```

<node> ...
<hierarchy>N-2-2</hierarchy>
<cpu>
  <type>Intel Q9450
  <frequency>2660</frequency>
  <SIMD>SSE4.1</SIMD>
  ...
  <cache>
    <id>2</id>
    <level>2</level>
    <count>2</count>
    ...
    <shared>true</shared>
    <sharedatlevel>1</sharedatlevel>
    <upstream>
      <upstreamID>3</upstreamID>
      <minlatency>...</minlatency>
      <avglatency>...</avglatency>
      <maxlatency>...</maxlatency>
      <minbandwidth>...</minbandwidth>
    ...
    </upstream>
  </cache>
</cpu>
    
```

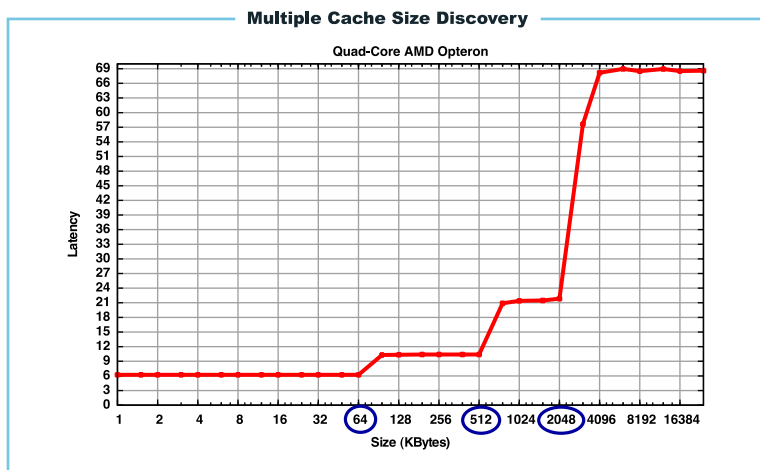
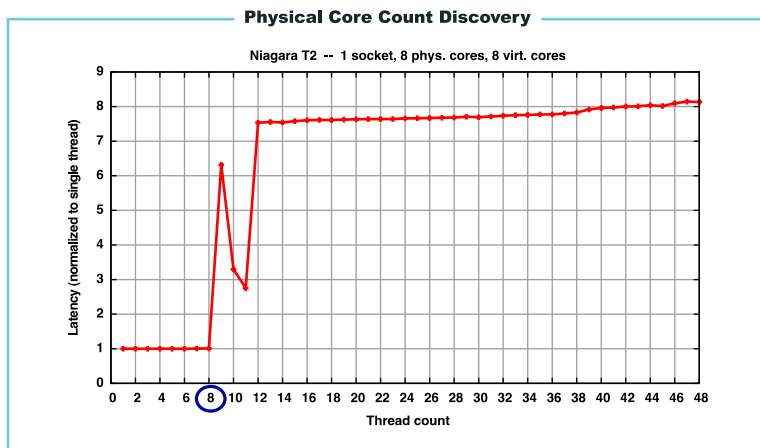
FIND OUT MORE AT <http://icl.eecs.utk.edu/blackjack/>

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The project's ultimate goals are to develop full metrics for evaluating the AACE development teams [T1], to implement representative applications and micro-benchmarks, to test and evaluate the productivity, correctness, and performance of multiple AACE prototype systems, to perform system characterizations, and to work with the T1 teams to develop a general characterization methodology and schema.

SYSTEM DISCOVERY MICRO-BENCHMARK EXAMPLES



POSSIBLE CHARACTERIZATION FILE ENTRIES

- PU info
 - Hierarchy
 - Frequency
 - Name
 - SIMD instructions
 - Pipeline depth
 - Register count/type
 - ...
- Cache hierarchy info
 - ID
 - Level
 - Count
 - Line Size
 - Size
 - Associativity
 - Is Shared [boolean]
 - Shared At Level
 - Upstream ID
 - Min, AVG, MAX Latency
 - Min, AVG, MAX Bandwidth
 - ...
- TLB info
 - Size [entries]
 - Miss latency
- RAM info
 - Size
 - {Min, AVG, MAX} Latency
 - {Min, AVG, MAX} Bandwidth
- Network info
 - Small Message Performance [100 Bytes]
 - Min, AVG, MAX Latency
 - Min, AVG, MAX Bandwidth
 - Medium Message Performance [4 KBytes]
 - Min, AVG, MAX Latency
 - Min, AVG, MAX Bandwidth
 - Large Message Performance [4 MBytes]
 - Min, AVG, MAX Latency
 - Min, AVG, MAX Bandwidth
 - RDMA [or other support for comm/comp overlapping]
 - Barrier, Broadcast cost
- OS/library info
 - malloc[]/free[]/alloca[] cost
 - Thread creation cost
 - Mutex/semaphore/cond. variable cost
 - Context switch delay
 - Scheduler tick

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