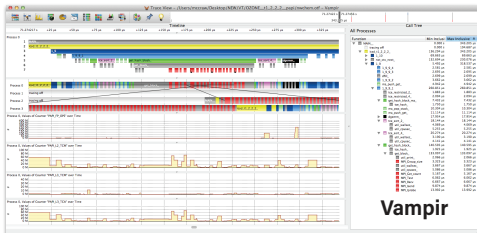


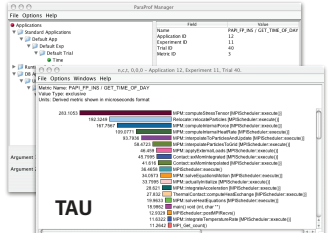
PAPI

THE PERFORMANCE APPLICATION PROGRAMMING INTERFACE

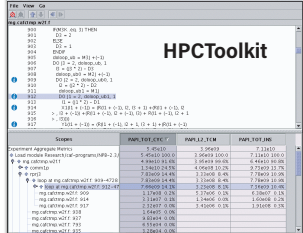
Performance Application Programming Interface (PAPI) provides a consistent interface (and methodology) for hardware performance counters found across a compute system: i. e., CPUs, GPUs, on- and off-chip memory, interconnects, I/O system, file system, and energy/power. PAPI enables software engineers to see, in near real time, the relationship between software performance and hardware events across the entire compute system.



Vampir



TAU



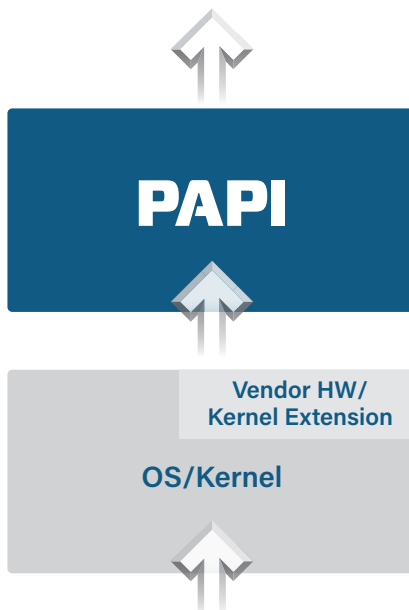
HPCToolkit

MORE
CrayPAT
ompP Tools
Open|SpeedShop
ParSEC
Scalasca
SCORE-P

PERFORMANCE ANALYSIS TOOLS

STANDARD FEATURES

- Standardized Performance Metrics
- Easy Access to Platform-Specific Metrics
- Multiplexed Event Measurement
- Dispatch on Overflow
- Overflow & Profiling on Multiple Simultaneous Events
- Bindings for C, Fortran and Matlab
- User Definable Metrics derived from Platform-Specific Metrics
- Support for Virtual Computing Environments
- Performance Counter Monitoring at Task Granularity for the ParSEC Dataflow Runtime
- Software-defined Event (SDE) support



SUPPORTED ARCHITECTURES

- AMD**
up to Zen3, power for Fam17h
GPUs MI50, MI60, MI100, power, temperature, fan
- ARM**
Cortex A7, A8, A9, A15, ARM64, ARM
uncore-support
- Cray**
Gemini and Aries interconnects |
RAPL power
- IBM**
Blue Gene Series, Q; 50-Torus, I/O
system, EMON power/energy
Power Series, PCP for POWER9-nest,
power monitoring & capping
- Infiniband**
- Intel**
Nehalem, Westmere, Sandy Bridge,
Ivy Bridge, Haswell, Haswell-EP,
Broadwell, Sky-, Kaby-, Cascade-,
Ice-lake, Knights Corner, Knights
Landing, Knights Mill | RAPL; power
capping, Power on Xeon Phi | Intel
RAPL (power/energy), power
capping capabilities (via
PAPI_write())
- Lustre**
- NVIDIA**
Tesla, Kepler, Maxwell, Pascal, Volta,
Turing, Ampere; support for multiple
GPUs | support for NVLink | NVIDIA
GPU support for power/energy
reading; power capping capabilities
(NVML)
- Virtual Environment**
VMWare, KVM



IN COLLABORATION WITH



SPONSORED BY



WITH SUPPORT FROM





Extending PAPI for ECP Applications

The Exa-PAPI project is developing new performance counter monitoring capabilities as well as power management support for novel and advanced ECP hardware, and software technologies.

Exa-PAPI builds upon classic-PAPI functionality and strengthens its path to exascale with a standard interface and methodology for using low-level performance counters in CPUs, GPUs, on/off-chip memory, interconnects, and the I/O system, including energy/power management.

In addition to providing hardware counter-based information, a standardizing layer for monitoring software-defined events (SDE) is being incorporated that exposes the internal behavior of runtime systems and libraries, such as communication and math libraries, to the applications. As a result, the notion of performance events is broadened from strictly hardware-related events to include software-based information. Enabling monitoring of both hardware and software events provides more flexibility to scientific application developers when capturing performance information.

Key Challenges

Widely deployed and widely used, PAPI has established itself as fundamental software infrastructure in every application domain where improving performance can be mission critical.

However, processor and system designs have been experiencing radical changes. Systems now combine multi-core CPUs and accelerators, shared and distributed memory, PCI-express and other interconnects, and power efficiency is emerging as a primary design constraint. These changes pose new challenges and bring new opportunities to PAPI. At the same time, the ever-increasing importance of communication and synchronization costs in parallel applications, as well as the emergence of task-based programming paradigms, pose challenges to the development of performance-critical applications and create a need for standardizing performance events that originate from various ECP software layers.

Solution Strategy

The Exa-PAPI team is preparing PAPI support to stand up to the challenges posed by exascale systems by:

- widening its applicability and providing robust support for exascale hardware resources;
- supporting finer-grain measurement and control of power, thus offering software developers a basic building block for dynamic application optimization under power constraints;
- extending PAPI to support software-defined events; and
- applying semantic analysis to hardware counters so that the application developer can better make sense of the ever-growing list of raw hardware performance events that can be measured during execution.

In summary, the team is channeling the monitoring capabilities of hardware counters, power usage, software-defined events into a robust PAPI software package.

RECENT PUBLICATIONS

Barry, D., Danalis, A., Jagode, H.
Effortless Monitoring of Arithmetic Intensity with PAPI's Counter Analysis Toolkit
13th International Workshop on Parallel Tools for High Performance Computing, Springer Nature Switzerland AG, C. Niethammer et al. (Eds.), pp. 1-25, 2020.

Jagode, H., A. Danalis, H. Anzt, J. Dongarra
PAPI Software-Defined Events for in-Depth Performance Analysis
The International Journal of High Performance Computing Applications 33, no. 6 (November 2019): 1113-27.
 doi:10.1177/10943342019846287.

Danalis, A., H. Jagode, T. Herault, P. Luszczek, J. Dongarra.
Software-defined Events through PAPI
24th International Workshop on High-Level Parallel Programming Models and Supportive Environments (HIPS), in conjunction with 33rd IEEE International Parallel & Distributed Processing Symposium (IPDPS), May 20-24, 2019, Rio de Janeiro, Brazil, pp. 1-10, 2019.

SPONSORED BY



Office of Science



This research was supported by the Exascale Computing Project (17-SC-20-SC), a collaborative effort of the U.S. Department of Energy Office of Science and the National Nuclear Security Administration.



EXASCALE COMPUTING PROJECT
<https://exascaleproject.org>

