Exploring Next Generation High Performance Computing Architecture for Post-Moore Era

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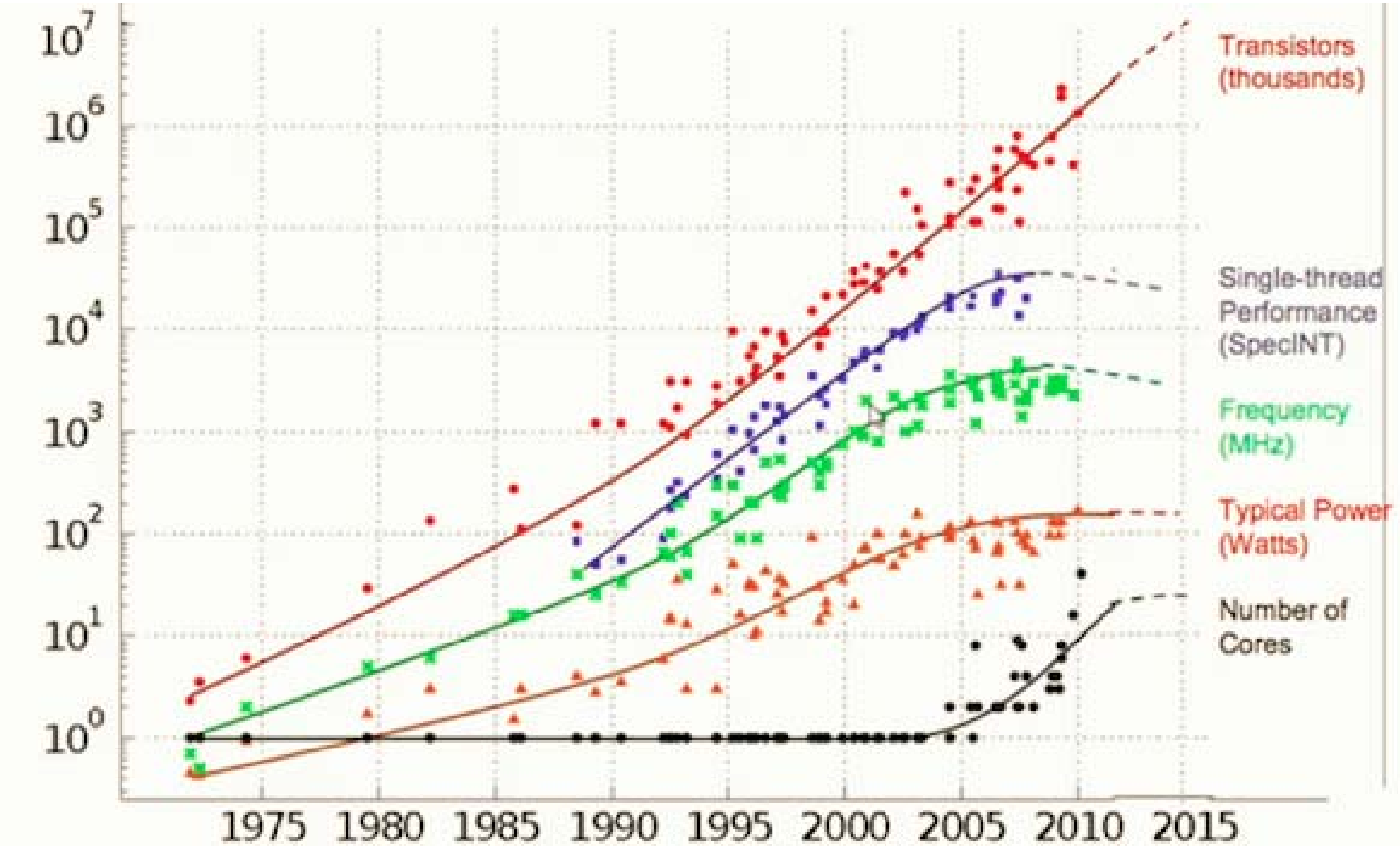
Moore's Law Slows Down and Will End



Courtesy: Chuck Moore, "DATA PROCESSING IN EXASCALE-CLASS COMPUTER SYSTEMS", The Salishan Conference on High Speed Computing, 2011.

Needs Innovative HPC system design for post-Moore era

Our Missions

- Exploring next generation HPC architecture for the Post-Moore era
  - Non-von Neumann architectures such as systolic arrays and neuro-morphic computers
  - Architectures that integrate various types of accelerators and next generation NVMs into a general-purpose processor
  - Advancing scientific simulations by accelerating machine learning computations
  - Hybrid computing architectures that combine the benefits of quantum computing and classical computing
  - Co-design evaluations of HPC architectures noted above as well as the co-design evaluations of algorithms that take advantage of them on the K computer and the post-K computer

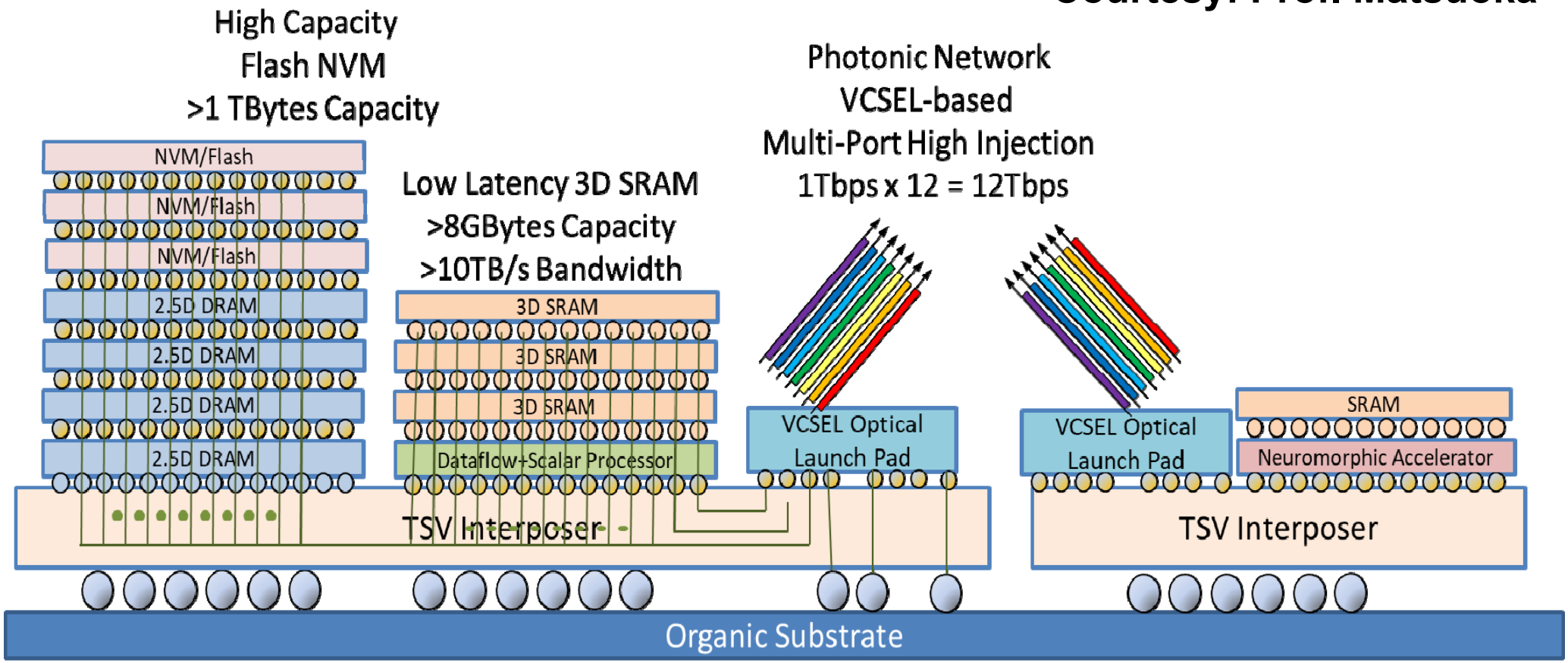
Towards Post-Moore Era

- Exploring HPC architectures in the Post-Moore Era
  - Wide variety of architectural / computing model choices
    - Types of execution units (Superscalar, SIMD, CGRA, …)
    - Types of memories (DRAM, NVM, 3D/2.5D stacking, deep hierarchy)
    - Types of interconnection networks (optics, topology, …)
    - Types of system architectures (NUMA, single-memory, …)
    - Types of devices technologies (CMOS, CNT, SFQ, 3D/2D, …)
    - Types of computing paradigms (traditional, quantum, AI, ising, …)
    - Types of architectural optimizations (low-precision, data-flow, …)

- Need an efficient methodology to evaluate post-Moore architectures and systems

Example Strawman Post-Moore Arch.

Courtesy: Prof. Matsuoka



- General purpose processor: Heterogeneous reconfigurable dataflow + scalar many-core processor, 200 Teraflops SFP, 20TeraFlops DFP
- Accelerators: Neural/Neuromorphic, Ising, Graph, etc.

- Direct Chip-Chip Interconnect with DWDM VCSEL micro-optics, 12Tbps injection bandwidth
- Low arity switches for multi-dimensional torus, multi-channel network injection ports

Methods of Architecture Exploration

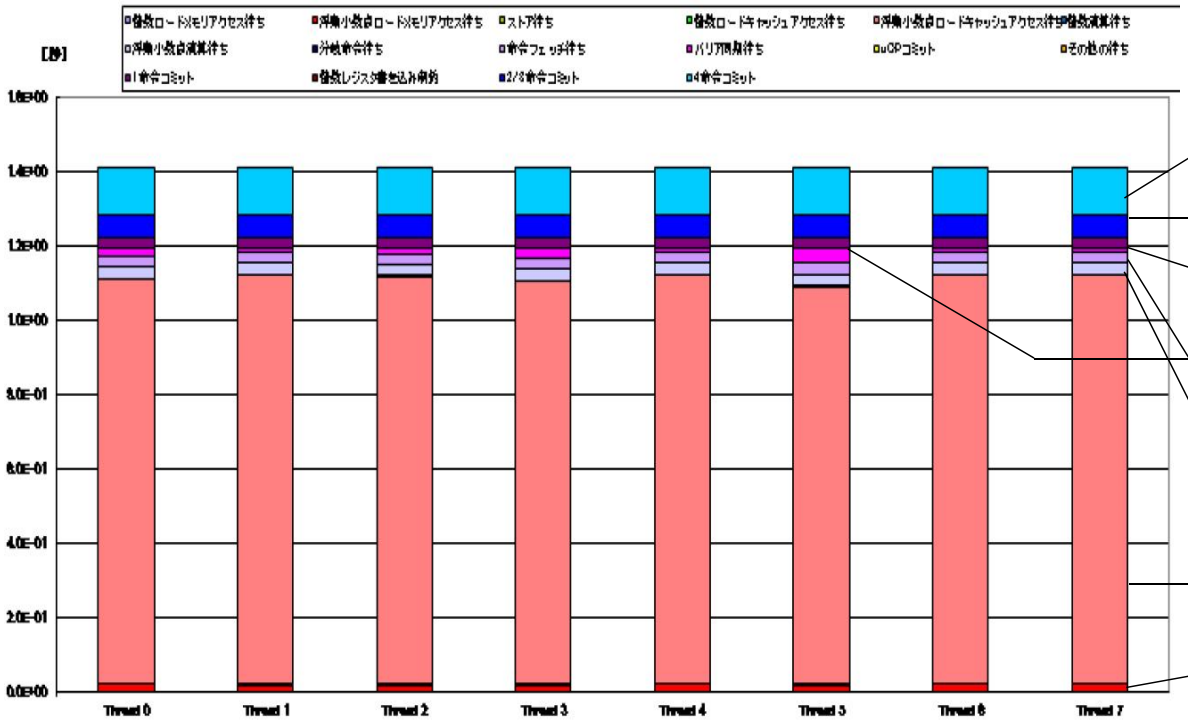
- Developing testbed systems (real silicon or FPGA)
  - Too costly and needs very long time
  - Sometimes impossible to use new devices
- Using cycle accurate architectural simulators
  - Easy to use and almost no $ cost
  - Sometimes too slow to evaluate benchmark programs
  - Still needs a large amount of engineering efforts to develop or modify a simulator for a given target architecture
- PMC based performance model (CPI stack analysis)
  - Almost no $ cost and very fast to estimate performance
  - Need to obtain PMC values in existing systems
  - Estimation accuracy depends on the model developed

Example of PMC-based Analysis

- Performance analysis tools in K-Computer
  - Developed by Fujitsu in collaboration with R-CCS
  - Obtains some PMCs in K-Computer

    % fapp -C -d pa1 -Hpa=1 mpiexec -n 8 ./a.out
  - Analyzes PMCs and generates execution cycle breakdown

    % fapppx -A -d pa1 -o output1.csv -tcsv -Hpa



4 instructions commit
2/3 instructions commit
1 instruction commit
Barrier synchronization wait
Instruction fetch wait
FP instruction exc. wait
FP cache access wait
FP memory access wait

Research Challenges

- Way to estimate wide variety of architectures
  - Scale each component according to expected BW/latency/size
    - Ex.) If cache latency becomes half, halves “cache access wait”

- Challenges
  - Obtain fine-grained CPI breakdown
  - Distinguish BW and latency contribution in each portion
  - Estimate overwraps when parameters change
  - Estimate hit rate for different size of caches

- Difficulties
  - How to estimate performance of new compute models
    - Non-von Neumann, Ising, …
  - How to expect the effect of programming model change
  - How to expect the compiler/code generation quality

Open for Collaboration

- Develop performance model and related tools for architectural exploration with PMCs
  - PMC-based CPI stack analysis combined with some simulations (cache, network, new devices, …)
  - Create a performance model taking into account BW/latency and overwraps
- Sharing PMC-data on several HPC systems for a set of pre-defined benchmark programs
  - Also validate performance model across HPC systems
- Create strawman architecture for post-Moore era
  - Includes sharing performance analysis results

Summary

- Towards post-Moore architecture exploration
  - Need an efficient architecture evaluation methodology
  - PMC-based CPI-stack performance analysis will be interesting approach
  - Requirement
    - Develop performance model and related tools
    - PMC data on wide variety of architectures and benchmarks
    - Parameters (throughput/latency/power/etc.) of future device technologies

- Your feedback is appreciated