Using SVE to Accelerate HPC Applications
A Mont-Blanc 2020 Perspective

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Vision: leverage the fast growing market of mobile technology for scientific computation

- 2012
- 2013
- 2014
- 2015
- 2016
- 2017
- 2018
- 2019
- 2020

**Mont-Blanc**

- Mont-Blanc 2
  - Proof of concept: HPC computing based on mobile embedded technology
  - Extend the concept and explore new possibilities
  - Design SoC
  - Develop IPs

- Mont-Blanc 3
  - Mont-Blanc 2020
  - Mont-Blanc 2020
  - Prepare an industrial solution
  - Test market acceptance

- Mont-Blanc 2020

Today

11th JLESC Workshop
Sept 10 2020
<table>
<thead>
<tr>
<th>Short Name</th>
<th>Country</th>
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<tbody>
<tr>
<td>Bull</td>
<td>FR</td>
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<tr>
<td>SemiDynamics</td>
<td>ES</td>
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<td>CEA</td>
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<td>BSC</td>
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<td>ARM</td>
<td>UK</td>
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<td>Juelich</td>
<td>DE</td>
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<td>Kalray</td>
<td>FR</td>
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MB2020 Objectives

- Define a low-power System-on-Chip (SoC) architecture targeting Exascale using Arm ISA
  - Leverage Arm’s strong technological relevance covering embedded to high end solutions
  - dynamic ecosystem, needed to deliver the system software and applications mandatory for successful market acceptance.

- To design, implement and leverage new technologies to improve the performance, power efficiency, reliability and security of the processor:
  - Exploit SVE compute units
  - specific Network-on-Chip (NoC) with high bandwidth and low power characteristics
  - specific SoC Power Management controller
  - innovative packaging technologies
  - state of the art silicon process

- To improve on the economic sustainability of processor development through a modular design that allows to retarget the SoC for different markets
Requirements for SVE: Design-space exploration

Explore hardware trade-offs

- Different vector lengths (128 to 2048 bits)
  - Off-chip memory bandwidth demands
    - Pin-based with DDR interfaces
    - Silicon interposer with HBM interfaces
- Sizing of key core structures – e.g., load/store queue
- Number of vector units – i.e., 2 x 256bit vs. 1 x 512bit
- Recommended memory bandwidth per core

Characterize performance of applications

- Demanded bytes per floating point operation – operational intensity (OI)
  - End goal: Understand how applications perform under different vector lengths and memory bandwidth constrains
**Requirements for SVE – Simulation parameters**

- **Resemble architecture envisioned in MB2020**

- **Gem5 simulation parameters**

<table>
<thead>
<tr>
<th>Description</th>
<th>Processor size</th>
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<tbody>
<tr>
<td>Cores</td>
<td>8 cores - 2 clusters of 4 cores each</td>
</tr>
<tr>
<td>L1I</td>
<td>64KB, 4-way, 2 cycle, 8MSHR</td>
</tr>
<tr>
<td>L1D</td>
<td>64KB, 4-way, 2 cycle, 24MSHR</td>
</tr>
<tr>
<td>L2 (private)</td>
<td>256KB, 2-way, 7 cycle, 24MSHR, stride prefetcher</td>
</tr>
<tr>
<td>Last-level Cache</td>
<td>16MB in 8 banks, 16-way, 20 cycles, 64MSHR</td>
</tr>
<tr>
<td>NoC</td>
<td>Coherent crossbar, 128-bit wide, 2 cycles</td>
</tr>
<tr>
<td>Main memory</td>
<td>4 DDR4-2400, 2 ranks/channel, 16 banks/rank, 8KB row-buffer 76.8 GB/s peak bandwidth</td>
</tr>
<tr>
<td></td>
<td>1 HBM stack, 8 channels/stack 128-bit wide, 8 banks/channel 128 GB/s peak bandwidth</td>
</tr>
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## Simulate a representative subset of the RAJAPerf loops
- Good auto-vectorization coverage

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Description</th>
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<tbody>
<tr>
<td>MULADDSUB</td>
<td>Simple synthetic loop for quick testing</td>
</tr>
<tr>
<td>HYDRO_1D</td>
<td>Main computational loop of the HYDRO application</td>
</tr>
<tr>
<td>EOS</td>
<td>Calculates the equation of state</td>
</tr>
<tr>
<td>INT_PREDICTOR</td>
<td>Integral predictor</td>
</tr>
<tr>
<td>ENERGY</td>
<td>Kernel to calculate energy states, extracted from an LLNL application</td>
</tr>
<tr>
<td>PRESSURE</td>
<td>Kernel to calculate pressure in a system, extracted from an LLNL application</td>
</tr>
<tr>
<td>FIR</td>
<td>Finite impulse filter, extracted from an LLNL application</td>
</tr>
<tr>
<td>LTIMES</td>
<td>Kernel extracted from an LLNL application</td>
</tr>
<tr>
<td>Stream-DOT</td>
<td>Stream benchmark, dot-product version</td>
</tr>
<tr>
<td>VOL3D</td>
<td>Kernel to calculate a 3D volume, extracted from an LLNL application</td>
</tr>
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</table>
Requirements for SVE – Vector length results (HBM)

- **Peak performance (compute ceilings)**
  - Peak SVE128 = 2GHz (cycles/s) × 8 (#cores) × 2 (flop/instr) × 2 (instr/cycle) = 64GFlops/s

- **Memory ceilings:**
  - Peak 128 GB/s
  - 16GB/s per core

- **Operational intensity**
  - Most benchmarks <1
  - Common values

- **HBM improves SVE scalability**
  - Memory bound benchmarks benefit greatly
  - EOS shows significantly better performance with SVE256

- **SVE 256 likely to be the best candidate**
  - Need at least OI == 2 to reach peak SVE 512 bit performance
Requirements for SVE – Summary of Requirements

Summary

- Use of HBM technology mandatory to scale to more than 8 cores per socket
- Recommend the use of SVE 256 or SVE 512 bits
  - SVE 512bits starts to be beneficial with OI > 1.5
  - SVE 512bits offers marginal benefits for OI < 1
- Contemporary aggressive OoO HW structures sufficient for SVE 256 & 512 bits
  - 48 LQ, 48SQ, 92 IQ, 192 ROB
  - 33% larger HW structures offer modest improvements – 17% max. 5% avg.
- We recommend a minimum of 16GB/s of off-chip memory bw per core
Next steps

- Look at a wider range of benchmarks
  - HACCKernels, HPCG, MiniAMR, SWFFT, XSbench, ...

- Validate simulations results vs Fujitsu’s A64FX processor
  - Issues with cluster installation at BSC (affected by covid19)
  - Reproduce RajaPerf performance figures with 256- and 512-bit SVE
  - Extend to other benchmarks of interest

- Evaluate large-scale applications on Fujitsu’s A64FX processor
  - HPC
  - Bioinformatics applications: genomics mappers and variant calling

- Interested in collaborating with other JLESC partners in that direction!
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