11th JLESC BoS:

Heterogeneous and reconfigurable architectures for the future of computing

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Xavier Martorell, Daniel Jimenez, Carlos Alvarez Martinez (BSC)

Agenda

- **Opening, and introduction of the FPGA-related project**
- **Talks (15min + 5min Q&A) x 5**
- **Panel Discussions**
- **Closing**

- **Speakers / Panelists**
  - ✔ Tomohiro Ueno, RIKEN, Japan
  - ✔ Jinpil Lee, RIKEN, Japan
  - ✔ Hal Finkel, ANL, USA
  - ✔ Carlos Alvarez, UPC and BSC, Spain
  - ✔ Christian Plessl, Paderborn University, Germany

Overview of this BoS

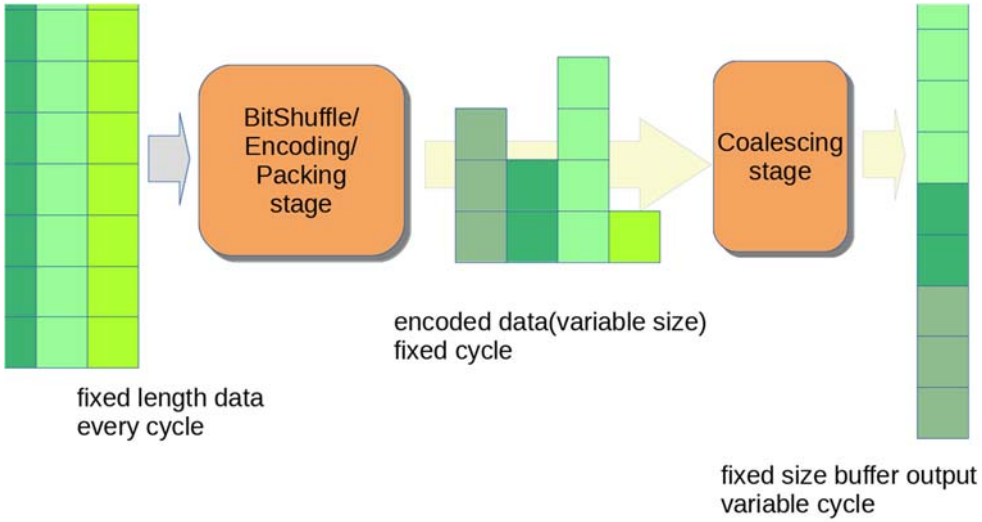
Title: Heterogeneous and reconfigurable architectures for the future of computing

- The forthcoming end of Moore's law encourages us to challenge new approaches for the future of computing.
- One of the promising approaches is heterogeneous and reconfigurable architecture with reconfigurable devices such as FPGAs and CGRA processors.
- In this BoS, we will discuss subjects and opportunities related to the new architectures with talks on recent research activities.

On-going FPGA-related Project

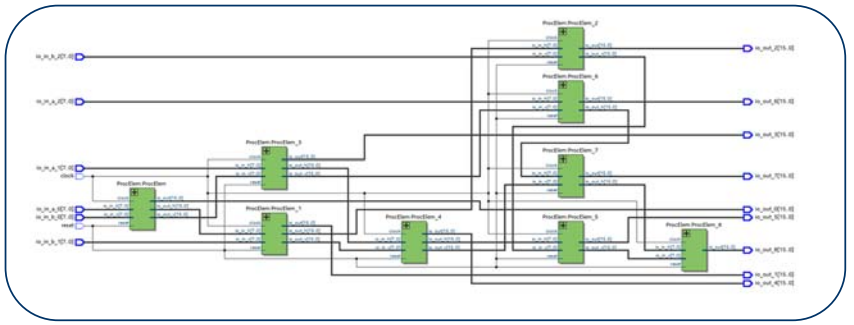
- **Project: Evaluating high-level programming models for FPGA platforms**
  - https://jlesc.github.io/projects/fpga_project/
- **Objective**
  - ✔ We focus on node-level parallelism; and our objective is to demonstrate, for a set of JLESC applications accelerated with emerging high-level synthesis technology, significant performance/watt improvement compared with CPUs and GPUs of the comparable technology.
- **Members**
  - ✔ Kazutomo Yoshii, Zheming Jin, Hal Finkel, Franck Cappello (ANL)
  - ✔ Xavier Martorell, Carlos Alvarez, Daniel Jimenez-Gonzalez, Osman Unsal (BSC)
  - ✔ Eric Rutten (INRIA)
  - ✔ Kentaro Sano (R-CCS)
- **Progress?**

Progress in ANL



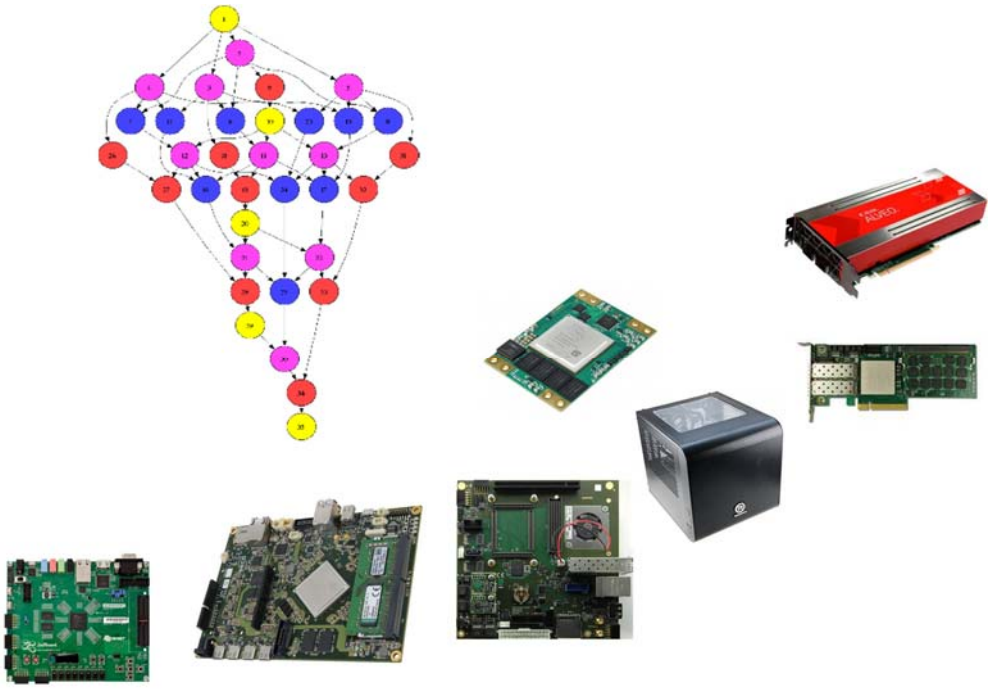
Evaluation of Hardware Construction Language

- **Exploring Chisel**
  - ✔ emerging domain specific language for describing synthesizable circuits
  - ✔ middle ground between hardware description language and high-level synthesis
  - ✔ leveraging the power of Scala
    - ➢ functional, object oriented language
  - ✔ seamless integration of testbench and cycle accurate simulator
  - ✔ fully open-source and gaining popularity due to RISC-V
- **Developing generator codes for stream compressors, systolic architecture, etc**
  - ✔ JINST journal paper accepted



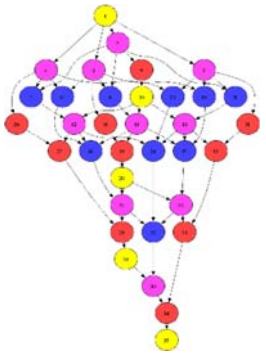
CHISEL

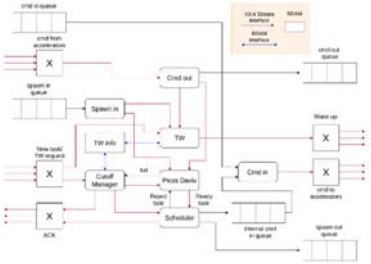
Progress in BSC

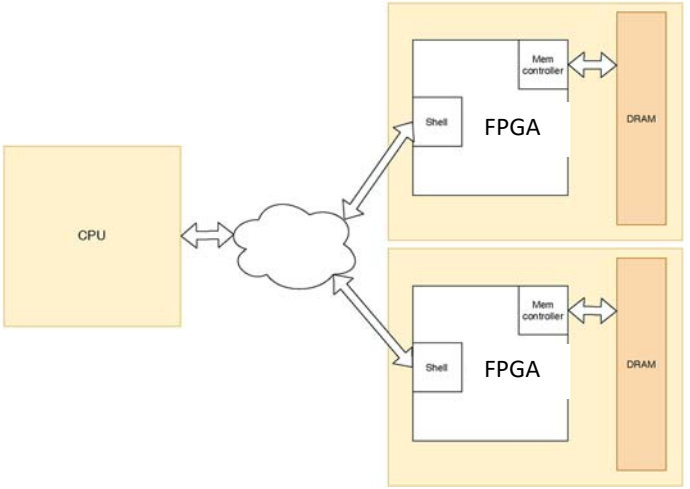


OmpSs@FPGA

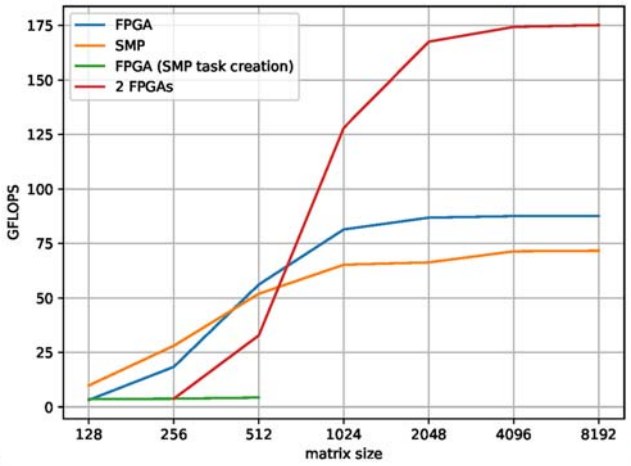
```
void cholesky(float *A[NT][NT]) {
   for (int k=0; k<NT; k++) {
      #pragma omp task inout(A[k][k])
      spotrf( A[k][k] ) ;
      for (int i=k+1; i<NT; i++) {
         #pragma omp task in(A[k][k]) inout(A[k][i])
         strsm( A[k][k], A[k][i] );
      }
      for (i=k+1; i<NT; i++) {
         for (int j=k+1; j<i; j++) {
            #pragma omp task in(A[k][i], A[k][j]) inout(A[j][i])
            sgemm( A[k][i], A[k][j], A[j][i] );
         }
         #pragma omp task in(A[k][i]) inout(A[i][i])
         ssyrk( A[k][i], A[i][i] );
      }
   }
}
```





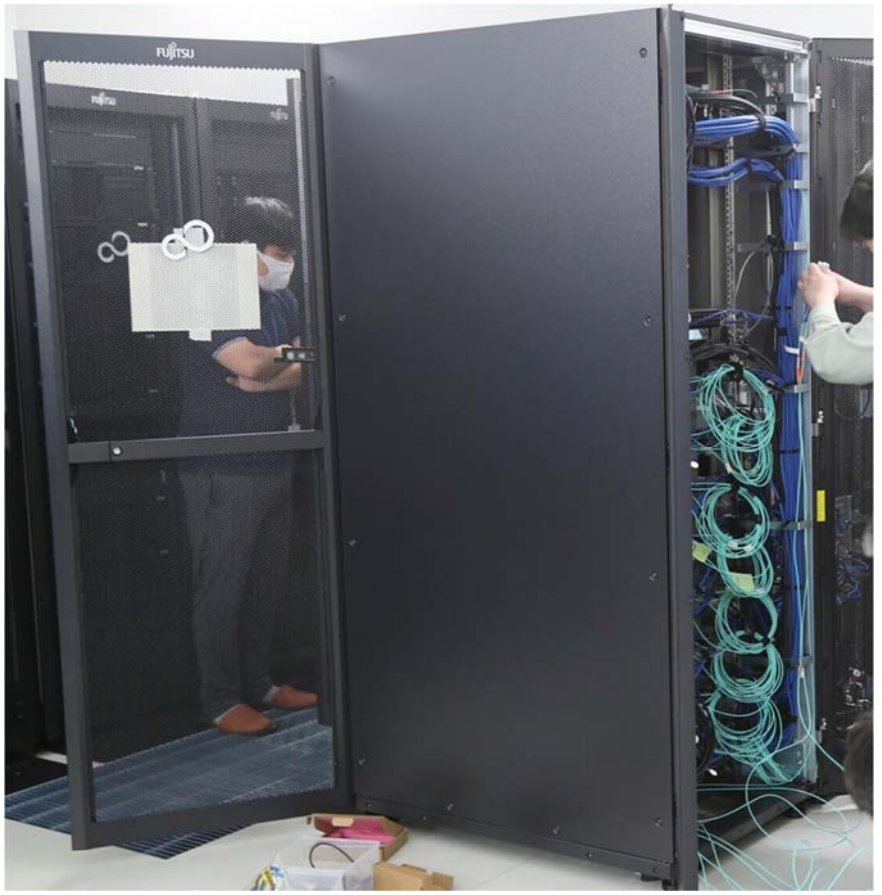


Matrix multiply - GFlops

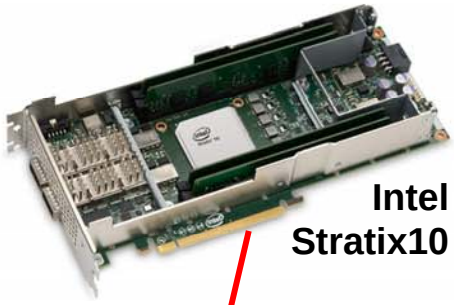


FPGA execution distribution over 2 FPGAs scales with resources
SMP managing is not an option over network
Faster than SMP and than using 1 FPGA

Progress in RIKEN



ESSPER: Elastic and Scalable System for High-Performance Reconfigurable Computing



Prototype of FPGA cluster

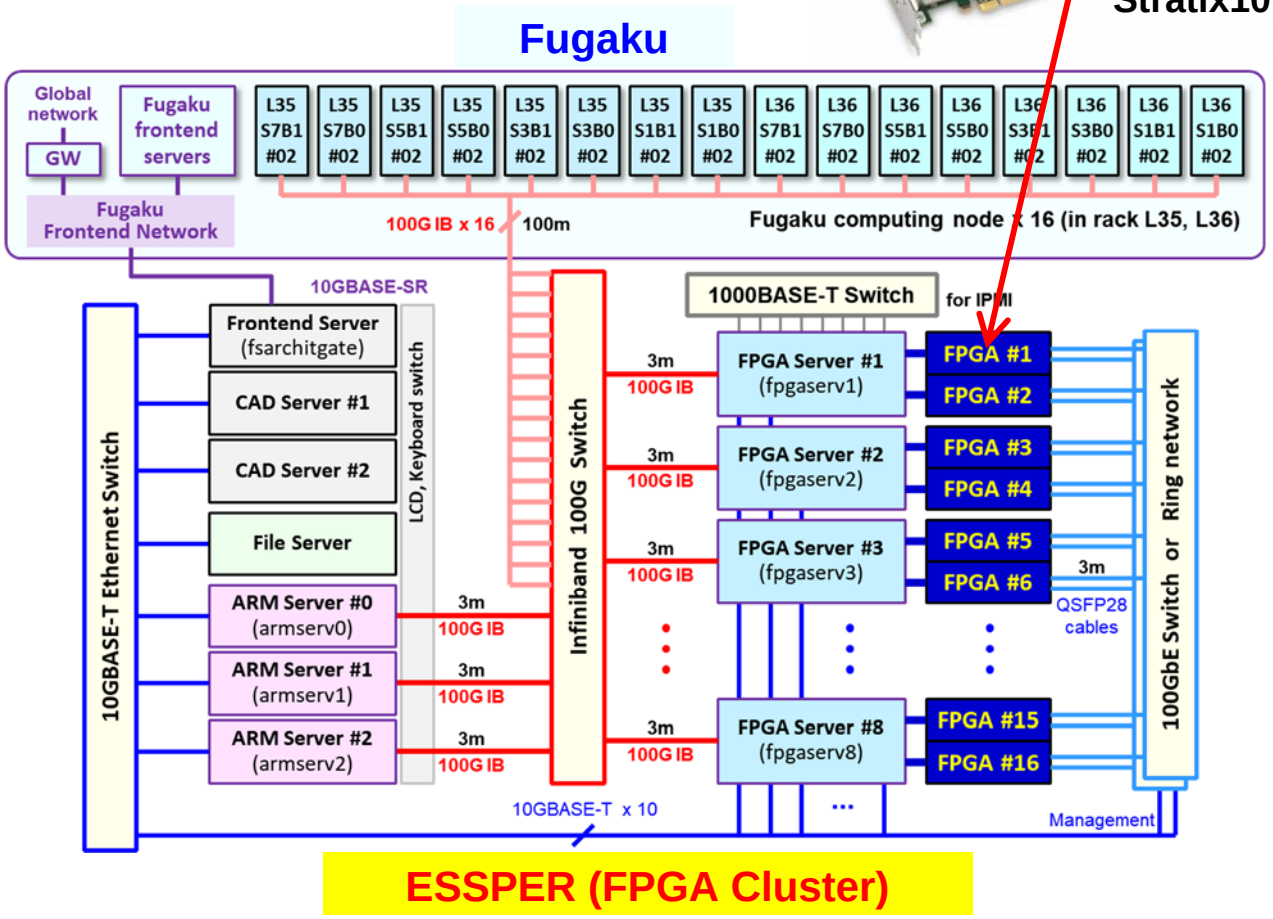
- ✔ Experiment to evaluate additional value of Fugaku
- ✔ Connected to some I/O nodes of Fugaku

Developed

- ✔ FPGA Shell with 100G links
- ✔ Remote-OPAE (sw bridge for FPGA driver)
- ✔ FPGA Shell class (HW abstraction)

On-going / Future plan

- ✔ FPGA Shell with 100G Ether
- ✔ Resource & network manager software
- ✔ Development of Benchmarks using HLS: 3DFFT, Genome, Graph, Clustering (SOM)



Panel Discussion : Questions from organizers

- **What do you envision the future reconfigurable architecture** that will drastically accelerate your workloads?
- **On what areas are you currently using** (or planning to use) **reconfigurable architecture?** (e.g., bioinformatics, 5G, physics experiments, HPC, Databases, AI, network acceleration, etc)?
- **Any expectations for (near-)future reconfigurable devices, boards, cloud services?** (Intel FPGAs, Xilinx FPGAs/ACAPs, etc.) -- what do you want to have/use?
- **What kind of partners do you need** for research collaborations?
- **What can you provide to users/app developers** for collaborations?
- **What are missing** (then we need to have) **to make FPGA-based collaborations realistic?**

Thank you!